UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,852	06/30/2000	Kiran A. Padwekar	042390.P5563	1971

7590 07/03/2003

Michael A DeSanctis
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,852	PADWEKAR, KIRAN A.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2000 and 12 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Declaration as received on 12 March 2001 and Extension of Time as received on 12 March 2001.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "100" has been used to designate both a simplified instruction pipeline and a computer system. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Figures 1 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 130 on page 2, line 10; 400 on page 9 and 10; and 523 on page 13, line 6. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 5, element 553 and Figure 6, elements 602, 609, and 612. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The disclosure is objected to because of the following informalities: Please correct page 4, line 4 from "The LLR bits 220 are used by the branch" to read --The LRR buts 220 are used by the branch--. Please correct on page 14, line 22 from "Figure 6is a flow diagram..." to read --Figure 6 is a flow diagram...--. Appropriate correction is required.

Claim Objections

8. Claims 3 and 8 are objected to because of the following informalities: Please correct claim 3 from "The method of claim 1, wherein the line has a corresponding a pattern table. and wherein said speculatively updating branch data comprises updating the pattern table." to read --The method of claim 1, wherein the line has a corresponding pattern table and wherein said speculatively updating branch data comprises updating the pattern table--. Please correct claim 8, line 7 from "speculatively allocating a second branch entry for the conditional branch in a the" to read --speculatively allocating a second branch entry for the conditional branch in the--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-2, 4, 7, 8-11, 14-17, and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., U.S. Patent Number 5,515,518 (herein referred to as Stiles) in view of Karp et al., U.S. 6,321,328 (herein referred to as Karp).

11. Referring to claim 1, Stiles has taught a method comprising maintaining speculative branch data for in-flight branches in a speculative branch target buffer (SBTB) cache by

a. Speculatively allocating a branch entry in a line of the SBTB after decoding an instruction containing a branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28),

b. Speculatively updating branch data associated with the branch entry after branch prediction has been completed for the branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28), and

c. Correcting the branch data (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

12. Stiles has not explicitly taught correcting the branch data after the branch has been executed. However, Stiles has taught correcting the branch data during the execution of the branch instruction. Karp has taught correcting speculative data in a cache after the instruction has been executed (Karp Abstract and column 2, lines 1-55). As Karp has taught, and is known to those of ordinary skill in the art, updating the data after it has been executed and committed

ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

13. Referring to claim 2, Stiles has taught the method:

a. Wherein the branch data includes a speculative history field representing the Speculative taken or not-taken history of the branch for a predetermined window of executions of the branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28), and

b. Wherein said speculatively updating branch data comprises updating the speculative history field to reflect the taken or not-taken status of its most recent execution (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

14. Referring to claim 4, Stiles has taught wherein the branch comprises a conditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

15. Referring to claim 7, wherein the branch comprises an unconditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

16. Referring to claims 8 and 14, Stiles has taught a method comprising:

a. Speculatively allocating a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional

branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28);

b. Speculatively allocating a second branch entry for the conditional branch in a the SBTB (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28)

c. Subsequently performing branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

17. Stiles has not explicitly taught:

a. Speculatively allocating responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch (Karp Abstract and column 2, lines 1-55) and

b. Allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch (Karp Abstract and column 2, lines 1-55).

18. However, Stiles has taught allocating branch entries (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28). Karp has taught:

a. Speculatively allocating responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch (Karp Abstract and column 2, lines 1-55) and

b. Allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch (Karp Abstract and column 2, lines 1-55).

19. Karp has taught, and a person of ordinary skill in the art would recognize, allocating data into a cache to decrease the stalls needed to access this information when it is not found in the current cache and updating the data after it has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

20. Referring to claims 9 and 15, Stiles has taught speculatively updating branch data associated with the first branch entry after said performing branch prediction for the conditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

21. Referring to claims 10 and 11, Stiles has taught a branch prediction circuit comprising:

a. Speculative branch target buffer (SBTB) means for maintaining speculative branch data (Applicant's claim 10) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28)

b. Architectural branch target buffer (ABTB) means, coupled to the SBTB means, for maintaining architectural branch data for branches (Applicant's claim 10) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28); and

c. Target address generation means coupled to both the SBTB means and the ABTB means for determining a predicted target address based upon the speculative branch data and the architectural branch data (Applicant's claim 10) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

22. Stiles has not explicitly taught:

a. SBTB associated with in-flight branches (Applicant's claim 10);

b. ABTB corresponding to retired instructions (Applicant's claim 10); and

c. Wherein the SBTB means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 11).

23. However, Stiles has taught two caches (Stiles column 3, line 18 thru column 4, line 28), but not when they are exactly accessed and what type of cache they are. Karp has explicitly taught:

a. A first cache associated with in-flight instructions (Applicant's claim 10) (Karp Abstract and column 2, lines 1-55);

b. A second cache corresponding to retired instructions (Applicant's claim 10) (Karp Abstract and column 2, lines 1-55); and

c. Wherein the first cache means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 11) (Karp Abstract and column 2, lines 1-55).

24. Karp has taught, and a person of ordinary skill in the art would recognize, allocating speculative data into a first cache to decrease the stalls needed to access this information when it

is not found in the second cache and entering the data into the second cache after the instruction has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

25. Referring to claims 16 and 17, Stiles has taught a branch prediction circuit comprising:

a. A speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes (Applicant's claim 16) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28) and

b. An architectural branch target buffer (ABTB) cache, coupled to the SBTB cache, the ABTB cache having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes (Applicant's claim 16) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

26. Stiles has not explicitly taught:

a. SBTB associated with in-flight branches (Applicant's claim 10);

b. ABTB associated to retired instructions (Applicant's claim 16); and

c. Wherein the first cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 17).

27. However, Stiles has taught two caches (Stiles column 3, line 18 thru column 4, line 28), but not when they are exactly accessed and what type of cache they are. Karp has explicitly taught:

a. A first cache associated with in-flight instructions (Applicant's claim 116) (Karp Abstract and column 2, lines 1-55);

b. A second cache associated to retired instructions (Applicant's claim 16) (Karp Abstract and column 2, lines 1-55); and

c. Wherein the first cache means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 17) (Karp Abstract and column 2, lines 1-55).

28. Karp has taught, and a person of ordinary skill in the art would recognize, allocating speculative data into a first cache to decrease the stalls needed to access this information when it is not found in the second cache and entering the data into the second cache after the instruction has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively

allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

29. Referring to claims 21 and 22, Stiles has taught a processor comprising:

a. A fetch unit to speculatively retrieve instruction data for processing by an instruction pipeline (Applicant's claim 21) (Stiles column 4, lines 62-66 and Figure 2); and

b. A branch prediction circuit, coupled to the fetch unit, to predict final target addresses for branch instructions contained within the instruction data (Applicant's claim 21) (Stiles column 4, lines 62-66 and Figure 2), the branch prediction circuit including:

i. A speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes (Applicant's claim 21) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28) and

ii. An architectural branch target buffer (A.BTB) cache, coupled to the SBTB cache, the ABTB having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes (Applicant's claim 21) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

30. Stiles has not explicitly taught:

a. SBTB associated with in-flight branches (Applicant's claim 21);

b. ABTB associated to retired instructions (Applicant's claim 21); and

c. Wherein the first cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 22).

31. However, Stiles has taught two caches (Stiles column 3, line 18 thru column 4, line 28), but not when they are exactly accessed and what type of cache they are. Karp has explicitly taught:

a. A first cache associated with in-flight instructions (Applicant's claim 21) (Karp Abstract and column 2, lines 1-55);

b. A second cache associated to retired instructions (Applicant's claim 21) (Karp Abstract and column 2, lines 1-55); and

c. Wherein the first cache means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 22) (Karp Abstract and column 2, lines 1-55).

32. Karp has taught and a person of ordinary skill in the art would recognize allocating speculative data into a first cache to decrease the stalls needed to access this information when it is not found in the second cache and entering the data into the second cache after the instruction has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would recognize that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively

allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

33. Claims 3, 5-6, 12-13, and 18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., U.S. Patent Number 5,515,518 (herein referred to as Stiles) in view of Karp et al., U.S. 6,321,328 (herein referred to as Karp) as applied to claims 1, 10, and 16 above, and further in view of Applicant's admitted prior art in the Background of the Invention (herein referred to as Prior Art).

34. Referring to claim 3, Stiles has taught the method wherein said speculatively updating branch data comprises updating the pattern table (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28). Stiles has not explicitly taught wherein the line has a corresponding a pattern table. However, Stiles has taught retaining information related to prior processing of branch instructions and using this information to predict the branch instruction. Prior Art has taught wherein the line has a corresponding a pattern table (Prior Art page 4, lines 1-4 and Figure 2). As taught in Prior Art, and known by one of ordinary skill in the art, the branch pattern table is used for predicting the outcome of conditional branch instructions in a line of branch entries (Prior Art page 4, lines 1-4 and Figure 2). A person of ordinary skill in the art would realize that a pattern table would be used in Stiles as a way to predict the outcome of conditional branch instructions and increase the speed of the processor by reducing the delay due to processing these branches due to the prediction. A person of ordinary skill in the art would have recognized that the pattern table is a commonly known method for predicting the outcome of conditional branch instructions. Therefore, it would have been obvious to a person of

ordinary skill in the art at the time this invention was made to incorporate the pattern table of Prior Art in the device of Stiles to increase the speed of the processor.

35. Referring to claims 5 and 6, Stiles has not explicitly taught the method:

a. Wherein the branch comprises a return from a subroutine (Applicant's claim 5)

b. Wherein the branch comprises a call to a subroutine (Applicant's claim 6)

36. However, Stiles has taught that his device applies to branches in general, branches of all types (Stiles column 1, lines 22-25). Prior Art has taught:

a. Wherein the branch comprises a return from a subroutine (Prior Art Page 4, lines 12-14) and

b. Wherein the branch comprises a call to a subroutine (Priori Art Page 4, lines 12-14).

37. Prior Art has taught, and it is known to one of ordinary skill in the art, that a call to and return from a subroutine are types of branches (Prior Art page 4, lines 12-14). A person of ordinary skill in the art would have recognized that a call to and return from a subroutine are types of branches. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a call to and return from a subroutine as taught by Prior Art in the device of Stiles since they are common types of branches.

38. Referring to claims 12, 13, and 18-20, Stiles has not taught:

a. Wherein the SBTB means includes a single read port and a single write port (Applicant's claim 12);

b. Wherein the SBTB means comprises a single-ported memory (Applicant's claim 13);

c. Wherein the SBTB cache is dual-ported (Applicant's claim 18);

d. Wherein the SBTB cache is single-ported (Applicant's claim 19); and

e. Wherein the ABTB cache is single-ported (Applicant's claim 20).

39. Prior Art has taught:

a. Wherein the SBTB means includes a single read port and a single write port (Applicant's claim 12) (Prior Art page 5, lines 1-5);

b. Wherein the SBTB means comprises a single-ported memory (Applicant's claim 13) (Prior Art page 5, lines 1-5);

c. Wherein the SBTB cache is dual-ported (Applicant's claim 18) (Prior Art page 5, lines 1-5);

d. Wherein the SBTB cache is single-ported (Applicant's claim 19) (Prior Art page 5, lines 1-5); and

e. Wherein the ABTB cache is single-ported (Applicant's claim 20) (Prior Art page 5, lines 1-5).

40. As stated in Prior Art and known to a person of ordinary skill in the art, the reading/writing ports allow the SBTB to be accessed by the various pipeline stages for information (Prior Art page 5, lines 1-5) and it is necessary for the information to be available to the rest of the device for it to function properly. A person of ordinary skill in the art would have recognized that the read/write ports allows the information to be accessed by the various pipeline stages and the rest of the device. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the read/write ports of Prior Art

in the device of Stiles to allow information to be accessed by the various pipeline stages and the rest of the device.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Jain et al., U.S. Patent Number 5,553,255, has taught a branch prediction unit with multiple units.

b. Gochman et al., U.S. Patent Number 5,842,008, has taught a branch prediction system with a branch target buffer with multiple banks.

c. Stiles et al., U.S. Patent Number 6,067,616, has taught a branch prediction system with multiple caches.

d. Arya, U.S. Patent Number 6,185,668, has taught a system with separate speculative and actual data files.

e. Yeh et al., U.S. Patent Number 6,553,488, has taught a branch predictor with multiple branch prediction tables.

f. McMahan U.S. Patent Number 5,732,253, has taught a branch processing unit with multiple caches.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

44. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

June 27, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100